Amendments to the Specification:

Please replace paragraph [028] with the following amended paragraph:

Another advantage to the data organization unit 180 of Figure 3 is that the number of lanes of data in each lane group 190-198 can be configured based on the frequency of the CCLK signal and the frequency of the system clock SCLK clocking data from the parallel to serial converter 182 as well as the width of the external bus 134 and possibly other factors. Therefore, a memory hub 140 may be designed with a CCLK frequency ~~dictaged~~dictated by advances in technology or specific characterists of an system, and the SCLK frequency may be dictated by it own design constraints, thus changing the frequency ratio of CCLK to the frequency of SCLK. Additionally, some memory hubs 140 may be designed with a wider bus 134 than others. However, the ability to vary the number of lane groups clocked out of the data organization unit 180 each CCLK cycle can accommodate these changes without changing circuitry within the memory hub 140. The data organization unit 180 can be programmed to output a specific number of lanes each CCLK cycle by suitable means, such as through an I/O port during initialization.